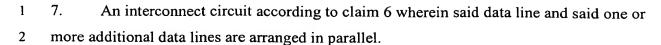


WHAT IS CLAIMED IS:

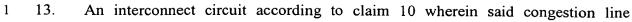
- 1 1. An interconnect circuit for transmitting data signals; said interconnect circuit comprising:
- a data line transmitting said data signals; and
- 4 a congestion line transmitting congestion signals;
- 5 wherein said data line selectively interrupts and reestablishes transmission of said
- data signals at selected portions of said data line responsive to said congestion
- 7 signals.
- 1 2. An interconnect circuit according to claim 1 wherein said data line transmits said
- 2 data signals and said congestion line transmits said congestion signals in opposite
- 3 directions.
- 1 3. An interconnect circuit according to claim 1 wherein said data line is adapted for
- 2 temporarily storing said data signals during periods in which said transmission of said
- data signals is selectively interrupted.
- 1 4. An interconnect circuit according to claim 1 further comprising:
- a first terminal inputting said data signals into said data line; and
- a second terminal receiving said data signals from said data line;
- 4 wherein said congestion signals are indicative of the status of said second
- 5 terminal.
- 1 5. An interconnect circuit according to claim 4 wherein said congestion line
- 2 transmits a congestion signal indicating that said second terminal cannot receive data at a
- 3 slower speed than said congestion line transmits a congestion signal indicating that said
- 4 second terminal can receive data.
- 1 6. An interconnect circuit according to claim 1 further comprising:
- one or more additional data lines transmitting additional data signals;
- 3 wherein said additional data lines selectively interrupt and reestablish
- 4 transmission of said additional data signals at selected portions of said additional
- 5 data lines responsive to said congestion signals.

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- 1 8. An interconnect circuit according to claim 1 wherein said data line comprises a
- 2 plurality of data driving circuits which selectively interrupt and reestablish transmission
- 3 of said data signals responsive to said congestion signals and wherein said plurality of
- 4 data driving circuits store said data signals temporarily when said transmission of said
- 5 data signals is interrupted.
- 1 9. An interconnect circuit according to claim 8 wherein said plurality of data driving
- 2 circuits are capable of arithmetical or logical functions.
- 1 10. An interconnect circuit according to claim 8 wherein said data line further 2 comprises:
- a first data driving circuit which interrupts transmission of said data signals responsive to a first congestion signal level and reestablishes transmission of said data signals responsive to a second congestion signal level; and
- a second data driving circuit which interrupts transmission of said data signals responsive to a third congestion signal level and reestablishes transmission of said data signals responsive to a fourth congestion signal level.
 - 11. An interconnect circuit according to claim 10 wherein said data line further comprises:
- a plurality of first data driving circuits which interrupt transmission of said data signals responsive to said first congestion signal level and reestablish transmission
- of said data signals responsive to said second congestion signal level; and
- a plurality of second data driving circuits which interrupt transmission of said data
- signals responsive to said third congestion signal level and reestablish
- 8 transmission of said data signals responsive to said fourth congestion signal level;
- wherein each of said plurality of first data driving circuits and each of said plurality of second data driving circuits are arranged in alternating fashion.
- 1 12. An interconnect circuit according to claim 10 wherein said congestion line
- 2 supplies said first congestion signal level to said first data driving circuit and said third
- 3 congestion signal level to said second data driving circuit.



- 2 supplies said second congestion signal level to said first data driving circuit and said
- 3 fourth congestion signal level to said second data driving circuit.
- 1 14. An interconnect circuit according to claim 10 wherein said first congestion signal
- 2 level is equal to said fourth congestion signal level and said second congestion signal
- 3 level is equal to said third congestion signal level.
- 1 15. An interconnect circuit comprising:
- a data line transmitting data signals from a first terminal to a second terminal; said
- data line comprising a plurality of data driving circuits selectively interrupting and
- 4 reestablishing transmission of said data signals responsive to congestion signals;
- 5 and
- a congestion line supplying said congestion signals to each of said plurality of
- 7 data driving circuits.
- 1 16. An interconnect circuit according to claim 15 wherein said congestion line
- 2 comprises a plurality of secondary driving circuits transmitting said congestion signals in
- 3 said congestion line in a direction opposite the direction of said transmission of said data
- 4 signals.
- 1 17. An interconnect circuit according to claim 15 wherein said congestion line
- 2 supplies said congestion signals to each of said plurality of data driving circuits in
- 3 sequence from said second terminal proceeding to said first terminal.
- 1 18. An interconnect circuit according to claim 15 wherein said congestion signals are
- 2 indicative of the status of said second terminal and wherein:
- 3 said plurality of data driving circuits interrupt transmission of said data signals
- 4 responsive to a first congestion signal indicating said second terminal is not
- 5 receiving data; and
- 6 said plurality of data driving circuits reestablish transmission of said data signals
- 7 responsive to a second congestion signal indicating said second terminal is
- 8 receiving data.
- 1 19. An interconnect circuit according to claim 18 wherein said first congestion signal
- 2 is transmitted through said congestion line at a slower speed than said second congestion
- 3 signal.

- 1 20. An interconnect circuit according to claim 16 wherein the number of said
- 2 secondary driving circuits is different from the number of said data driving circuits.
- 1 21. An interconnect circuit according to claim 15 further comprising:
- a plurality of additional data lines transmitting additional data signals from said
- 3 first terminal to said second terminal and selectively interrupting and
- 4 reestablishing transmission of said additional data signals responsive to said
- 5 congestion signals.
- 1 22. An interconnect circuit according to claim 21 wherein said data line and said
- 2 plurality of additional data lines are arranged in parallel.
- 1 23. An interconnect circuit according to claim 15 wherein said data driving circuits
- 2 are adapted to store said data signals temporarily during the period when said
- 3 transmission of said data signals is interrupted.
- 1 24. An interconnect circuit according to claim 15 wherein said data driving circuits
- 2 are capable of arithmetical or logical functions.
- 1 25. An interconnect circuit according to claim 15 wherein said congestion line
- 2 supplies said congestion signals at a first congestion signal level and a second congestion
- 3 signal level; said data line interrupting transmission of said data signals responsive to said
- 4 first congestion signal level and reestablishing transmission of said data signals
- 5 responsive to said second congestion signal level.
- 1 26. A method of transmitting data signals through an interconnect; said method
- 2 comprising:
- providing a data line for transmitting said data signals from a first terminal to a
- 4 second terminal through a plurality of data driving circuits;
- 5 providing a congestion line for transmitting congestion signals to each of said
- 6 plurality of data driving circuits; and
- selectively interrupting and reestablishing transmission of said data signals at said
- 8 plurality of data driving circuits responsive to said congestion signals.
- 1 27. A method according to claim 26 wherein said providing a congestion line further
- 2 comprises providing a plurality of secondary driving circuits for transmitting said

- 3 congestion signals in a direction opposite the direction of said transmission of said data
- 4 signals.
- 1 28. A method according to claim 26 wherein said providing a data line further
- 2 comprises enabling said plurality of data driving circuits to store said data signals
- 3 temporarily when said transmission of said data signals is interrupted.
- 1 29. A method according to claim 26 wherein said transmitting congestion signals
- 2 further comprises:
- 3 transmitting a first congestion signal indicating said second terminal is not
- 4 receiving data; and
- alternatively, transmitting a second congestion signal indicating said second
- 6 terminal is receiving data;
- 7 wherein said first congestion signal is transmitted at a slower speed than said
- 8 second congestion signal.
- 1 30. A method according to claim 26 further comprising:
- 2 providing a plurality of additional data lines for transmitting additional data
- 3 signals from said first terminal to said second terminal; and
- 4 selectively interrupting and reestablishing transmission of said additional data
- 5 signals responsive to said congestion signals.
- 1 31. A method according to claim 30 further comprising arranging said data line and
- 2 said plurality of additional data lines in parallel.
- 1 32. A method according to claim 26 wherein said providing a data line includes
- 2 providing said plurality of data driving circuits with arithmetical or logical function
- 3 capabilities.